MODULAR MULTILEVEL CONVERTER FED WITH WIND ENERGY FOR HIGH STEP-UP RATIO DC-DC CONVERSION

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Abstract—A modular multilevel dc–dc converter fed with wind source is depends upon the boost converter topology but here normal single switches are recouped with series of capacitor clamped submodules. In wind turbine interfaces and high voltage direct current systems high step-up ratio converters are used. The converter is operated in resonant mode with resonance between submodule capacitors and the arm inductor. The proposed converter may shows relatively huge losses because of the high ac current that resonates in the submodules, but wisely high efficiency was possible in high-voltage applications. A phase-shifted switching layout is applied such that there is a constant number, i.e., N, of submodules supporting the high voltage at a time. In this operation mode, the step-up ratio is dependent on the number of submodules and the inductor charging ratio. This converter gives the scalability without using a transformer and is able to give bidirectional power flow. An application example of a wind turbine interface with a 10:1 conversion ratio is validated in simulation.

I. INTRODUCTION

The harmonic content of the output voltage as compared with the traditional two-level converters the multilevel converters used for medium-voltage and high-voltage applications [1]–[4]. Multilevel converter schemes for dc–dc conversion are becoming popular [5] in renewable energy applications following the success of this approach in dc–ac conversion. The modular multilevel converter (MMC) is found to have more attractive features than the others. Diode-clamped converters have a large number of diodes required, and with the unbalancing issue, making the system impractical to implement. There are many different types of multilevel converters developed [6], which can be directly or indirectly used as step-up dc–dc converters. Conventional flying capacitor converters [7] require many capacitors connected in series. The total series capacitance is much smaller than that of a single one. Therefore, the total volume of capacitors required is quite high. Generalized multilevel converters can be used for maximum output voltage dc–dc conversion [8], [9], but the topology results in a large size when the step ratio is high. Other topologies such as input-parallel output-series (IPOS) converters [10] and switched capacitor converters have been proposed and developed for step-up dc–dc conversion [11]–[13].

Switched capacitor converters with series-parallel topologies are subject to incremental voltage stress either on the module switch or on the module capacitor. The highest voltage stress is close to the maximum output (high-side) dc voltage. The switched capacitor converters are also subject to high charge losses and overshoot currents. This problem can be mitigated by driving metal–oxide–semiconductor field-effect transistors (MOSFETs) with very high switching frequency. Therefore, in low-voltage condition switched capacitor converters are only used. A power-electronics-based Cockcroft–Walton multiplier has been demonstrated in [15]. This is a light and cheap solution for maximum voltage dc experiments when only unidirectional step-up conversion is required. A bidirectional medium voltage “ladder”-shaped dc–dc converter is proposed in [16], which can achieve a high step ratio. The advantage is that the converter does not require synchronization of switching between submodules. However, the current ratings in different submodules are not the same, and the inductor currents close to the low-voltage side are high.

Dc–dc conversion is used to the medium- and maximum voltage applications, MMCs used for are emerging technologies [5], [17]. These converters are based on conventional MMCs [18]–[20]. MMCs usually require a complicated balancing control scheme to maintain the voltage levels. However, they provide more than two levels and good waveform quality by using pwm controller. Cells with fault can also be bypassed while keeping the system operational. High modularity and redundancy are the main advantages of MMCs.

This paper presents a new topology and control scheme of a modular multilevel bidirectional dc–dc converter with ratio of maximum output voltage. There has been no direct and simple solution for large maximum output voltage of dc–dc conversion using the MMC approach. It is based on the conventional boost converter with groups of submodules placed in both the diode and switch positions. The proposed converter can achieve a high step ratio. Phase-shifted pulse width modulation (PWM) is used to achieve a high effective operating frequency for a given submodule switching frequency. The proposed converter is bidirectional and suitable for low-power dc–dc applications as it has the feature of modularity, simplicity, and flexibility. The configuration of the circuit and its operation principle are presented and verified by experimental results from a downscaled prototype.

II. BIDIRECTIONAL MODULAR MULTILEVEL DC–DC CONVERTERS

In converting a simple standard switched-mode circuit to a modular multilevel format, a variety of capacitor-clamped submodules are required. Fig. 1 shows clamped single switches that use the half-bridge configuration in which replacements for a single insulated-gate bipolar transistor (IGBT), a diode, and an IGBT with an anti parallel diode are illustrated. The ability to clamp the off-state voltage across a switch when a stack of
The most commonly used boost converter configuration. The number of upper deal, and the submodules are simultaneous (clamped diode) submodules in the upper

3) In steady state, the capacitor dc voltages are balanced.

A. System Configuration

The configuration of the maximum output voltage step-up conversion is provided to demonstrate the concept. The fig. 3 shows the most commonly used boost converter topology with a single IGBT and a single diode. The IGBT in the lower position is used for charging the input inductor L. The diode in the upper position of the circuit is automatically commutated on when the inductor is discharging current to the high-voltage capacitor CH. Applying active clamping (see Fig. 1) to the two switches, the modular multilevel unidirectional high voltage converter with two stacks of submodules is obtained as shown in Fig. 3(b). The number of the half-bridge (clamped IGBT) submodules in the lower position is M. The number of the chopper (clamped diode) submodules in the upper position is N. The output (high-side) voltage is approximately equal to the sum of capacitor voltages of the stack of submodules once duty cycles are accounted for. There will be small differences between the instantaneous voltage across the stack (as submodules switch) and the voltage across CH, and this is accommodated by including the small inductor Ls. A large capacitor Cl would normally be present at the input (low voltage) side. The step-down conversion is configured using the similar concept. The fig. 4 shows the circuit of the proposed converter for step-down operation.

B. Phase-Shift Control

The proposed converter has various operating modes resulting in different operating features and step-up ratios. Apart from the high voltage ratio operation mode, which is the focus of this paper, the converter can also be used for high step-down ratio dc–dc conversion providing power for an auxiliary electronic circuit in medium-voltage systems. Moreover, with similar numbers of submodules in the upper stack and the lower stack, the converter can also be used for low-step-ratio high-voltage dc–dc conversion. Phase-shifted PWM and fuzzy logic controller is used to control the modular multilevel step-up dc–dc converter. Phase-shifted PWM is arranged with a high duty cycle such that only one submodule capacitor at a time is out of the series connection, and thus, the step-up ratio of the circuit becomes dependent on the number of upper cells N. The

3. HIGH STEP-UP RATIO MODULAR MULTILEVEL DC–DC CONVERTER

This section describes the operation method for the proposed dc–dc converter. The analysis focuses on maximum output voltage dc–dc conversion. To simplify the analysis, the theoretical developments are based on the following assumptions.

1) The switches are ideal, and the submodules are identical.

2) The converter is lossless.

The classic bidirectional two-level dc–dc converter is shown in Fig. 2(a). The positive-clamping idea can also be applied to dc–dc converters. The upper IGBT in the half bridge is termed as clamping IGBT, whereas the lower IGBT is termed as clamped IGBT. It consists of an inductor on the low-voltage side, two IGBTs with antiparallel diodes, and capacitors on both input and output sides. The fig. 2 shows the replacing all the switches by series connected submodules with active clamping; the bidirectional buck–boost converter becomes the modular multilevel dc–dc converter. The number of upper submodules is not required to be the same as the number of the lower submodules; however, special operation techniques are required.

The switches is connected in series is crucial in forming MMC topologies. The MMC topology was generated by clamping the series-connected IGBTs in the conventional two-level inverter. With active clamping, each switch has a well-defined voltage and good sharing between submodules.

Fig. 2. Bidirectional dc–dc converters. (a) Conventional two-level dc–dc converter. (b) Novel modular multilevel dc–dc converter.

Fig. 3. Unidirectional step-up dc–dc converters. (a) Conventional boost converter. (b) Proposed modular multilevel step-up dc–dc converter.
effective frequency of this excitation is much higher than the frequency of switching of an individual cell.

Fig. 4. Unidirectional step-down dc–dc converters. (a) Conventional buck converter. (b) Proposed modular multilevel dc–dc converter.

To demonstrate the principle of interleaved PWM, a step up converter with four submodules in the diode position in the circuit of Fig. 3(b) is considered (N = 4). To ensure that either four or three submodules are injecting voltage at any time, each must be operated with a duty cycle above 75%. For illustration, 90% is used. One module could be used in the lower position operating at four times the switching frequency of the upper modules (to give the same effective frequency).

Instead, the system will be illustrated with two submodules in the lower position operating at twice the frequency of the upper submodules and with interleaved pulses. Assuming the submodule capacitor voltages to be constant, the key waveforms of the submodule voltages are shown in Fig. 5.

This guarantees an almost constant dc voltage with a small ripple on the high voltage side. It can be seen in Fig. 5 that the upper (clamped diode) cells are synchronously switched with the lower (clamped IGBT) cells so that the total voltage of the upper cells vN and lower cells vM are complementary. The equivalent operating frequency is four times the switching frequency of the upper cells (fe = 4fs) and is twice the switching frequency of the lower cells. As the frequency of the ripple on the high-voltage side is high, the passive components of the output filter do not need to be large.

The current waveforms in Fig. 5 will be explained with the high voltage operation. The step-down operation has the same stack voltage waveforms as that of the high voltage output conversion. This guarantees an almost constant dc voltage with a small ripple on the high voltage side. The time-domain waveforms of the stacks are shown in Fig. 6. In the step-down operation, the current directions and waveforms are different from that in the step-down operation. The operation of step-down conversion will be analyzed in detail in the following section.

C. High Conversion Ratio

Fig. 5. The proposed converter is aimed at high step-up ratio dc–dc conversion. The analysis of operation and conversion ratio will proceed by examining one equivalent cycle Te. Fig. 7 shows the detailed circuit diagrams with current paths highlighted for the two modes of the circuit. Mode 1 starts when the IGBT in Cell 4 is switched on and ends when the IGBT in Cell 1 switches off [see Fig. 7(a)]. The IGBT in Cell 1 switches off when the lower IGBT in Cell 5 switches off, and this defines the beginning of Mode 2 [see Fig. 7(b)]. Mode 2 ends when the IGBT of Cell 1 is switched on again. Modes 1 and 2 are analogous to the on- and off-states of the simple boost converter but with the difference that current can flow in both paths in both modes. The current flowing through the input inductor, upper cells (clamped diodes), and lower cells (clamped IGBTs) are defined as iL, iN, and iM, respectively.

The capacitors C1, C2, C3, and C4 are in series with the inductor Ls and the high-side (output) capacitor CH, and together, they form a resonant tank. In Mode 1, the current iL of inductor L is directly charged by the low-side (input) voltage vL via the IGBTs in Cell 5 and Cell 6. Because CH is large and the cell capacitors are smaller and placed in series, the resonance is dominated by the cell capacitors, and CH can be ignored. Therefore, the resonant frequency is

$$f_r = \frac{1}{2\pi \sqrt{L_s C/N}}$$  (1)
In the case of \( N = 4 \), \( \frac{1}{r_1} = \frac{1}{\pi} \sqrt{L_sC} \). When the converter enters Mode 2 from Mode 1, capacitor \( C_5 \) is connected into the circuit, whereas capacitor \( C_1 \) is out of series connection. The capacitors \( C_2, C_3, C_4, \) and \( C_5 \) are in resonant tank with \( L_s \) and \( C_H \). As the inductor \( L \) is relatively large, the current \( i_L \) is considered as from a current source. Therefore, the resonant frequency in Mode 2 is also dependent on four series-connected capacitors and the series inductor \( L_s \). When the lower (clamped IGBT) cells and the upper (clamped diode) cells use the same capacitors, the resonant frequency in Mode 2 is the same as that in Mode 1.

If the actual resonant frequency is slightly higher than \( f_r \), by the end of Mode 2, the current \( i_N \) reaches zero, and the circuit operates in discontinuous conduction mode (DCM). In Fig. 7(b), it can be seen that the current \( i_N \) cannot be negative in Mode 2 because one cell (Cell 1 in the figure) is acting as a diode.

The simulation result later in this paper will illustrate this. The current \( i_L \) is directly charged by the low-side voltage source. Meanwhile it begins model 1, the current \( i_N \) starts to resonate (starting from zero) with the frequency of \( f_r \). The current \( i_M \) is \( i_L \) minus \( i_N \). When the circuit enters Mode 2 from Mode 1, since \( v_C5 \) is higher than \( v_C1 \), the inductor current \( i_L \) reduces. As the circuit operates in DCM, before the end of the equivalent operating cycle, the current \( i_N \) falls to zero, and the current \( i_M \) is equal to \( i_L \) until a new cycle begins.

To obtain the voltage conversion ratio, the charging ratio \( d \) is defined as the time duration of Mode 1 relative to the period, i.e., \( T_e \) of the equivalent operating cycle. In steady state, the increase and decrease of \( i_L \) over a equivalent cycle \( T_e \) should be the same; hence,

\[
\frac{v_i T_e d}{L} = \frac{(v_{Cj} - v_L) T_e (1 - d)}{L} \quad (2)
\]

with \( j = 5 \) or \( j = 6 \). The capacitor voltages of the lower submodules can be written as

\[
v_{Cj} = \frac{v_L}{1 - d} \quad (3)
\]

The sum of average stack voltages \( v_N \) and \( v_M \) should be equal to the high-side voltage, i.e., \( v_H \), which yields

\[
v_H = \frac{N - 1 + d}{N} \sum_{j=1}^{N} v_{Cj} + \frac{1 - d}{M} \sum_{j=N+1}^{N+M} v_{Cj} \quad (4)
\]

Under ideal conditions, the capacitor voltages are balanced and equal to \( v_C \). The voltage conversion ratio can be derived by substituting (3) into (4), i.e.,

\[
\frac{v_H}{v_L} = \frac{N}{1 - d} \quad (5)
\]

It can be seen that without increasing \( d \), the conversion ratio can be increased by using higher numbers of upper submodules \( N \). In the case of \( N = 4 \), the conversion ratio is \( v_H/v_L = 4/(1 - d) \).

The low-side (input) inductor current \( i_L \) comprises a dc component and a sawtooth-shaped ripple. The current stresses in the converter should be estimated because it is important in determining the power losses and device ratings. The average current of \( i_L \) can be derived from the power consumed on the high voltage side. Here, it is assumed that the load dc current is \( I_0 \). Therefore,

\[
I_L = \frac{v_H}{v_L} I_0 \quad (6)
\]
The peak-to-peak ripple $\Delta I_L$ can be obtained from the charging time of inductor $L$, i.e.,

$$\Delta I_L = \frac{v_L T_e d}{L}. \quad (7)$$

The dc component of $iN$ goes on to feed the load, and its ac component circulates within the resonant tank. The current stress on the clamped-diode (upper) stack depends on $iN$. It will be assumed that the ac component of $iN$ is approximately sinusoidal with a root mean square (RMS) value of $IN1$ at the resonant frequency. The power transferred out of the clamped-diode (upper) stack by the flow of the dc current is

$$P_1 = (N - 1 + d) v_c I_o. \quad (8)$$

The peak-to-peak value of $vC$ on the other hand, the ac voltage of the upper stack is a square wave. Therefore, the RMS value of this square wave is $vC/2$. The power transferred into the stack by the sinusoidal resonant current interacting with the square-wave component of the stack voltage is

$$P_2 = \frac{v_c}{2} I_{N1}^2. \quad (9)$$

with $\lambda$ as the power factor for this voltage and current combination. The value of $\lambda$ can be obtained from numerical solutions. The maximum, i.e., $\lambda = 1$, is achieved when the charging ratio is $d = 0.5$. If the converter is lossless, the dc power and ac power of the upper stack should be equal. Therefore

$$I_{N1} = \frac{N - 1 + d}{\lambda} I_o. \quad (10)$$

After $iL$ and $iN$ are estimated, the current stress on the lower stack can be determined by $iM = iL - iN$. A rough estimation of $|iM| < |iL| + |iN|$ can also be used.

Although the converter is proposed for maximum output voltage dc–dc conversion, it also has the capability of step-down dc–dc conversion. Fig. 8 shows the detailed circuit diagrams with current paths highlighted for the two modes of the circuit. Mode 1 starts when the clamped IGBT in Cell 1 is switched on and ends when the clamped IGBT in Cell 1 is switched off [see Fig. 8(a)]. When the clamped IGBT in Cell 1 switches off and the clamping IGBT in Cell 5 switches off, the converter begins to enter Mode 2 [see Fig. 8(b)]. Mode 2 ends when the clamping IGBT of Cell 6 is switched off. For operation analysis, the current directions are defined opposite to the current directions in the step-up operation.

During Mode 1, the inductor $Ls$ and the capacitors $C2$, $C3$, and $C4$ are charged, and therefore, the clamped diodes in the lower cells are reverse-biased. As the voltage on the inductor $L$ in Mode 1 is higher than that in Mode 2, the current $iL$ of inductor $L$ is charged in Mode 1 and discharged in Mode 2. Meanwhile, the capacitors $C1$, $C2$, $C3$, and $C4$ in series with the inductor $Ls$ form a resonant tank to discharge the energy stored in the passive components from Mode 1. There is no current flowing through the lower stack. If the capacitor voltages are assumed to be constant, the currents $iL$ and $iN$ should linearly increase in Mode 1 and $iL$ equals $iN$. The slight increase in the cell capacitor voltages does not affect the wave shapes obviously. When the converter enters Mode 2 from Mode 1, all the cell capacitors in the upper stack are in series with the inductor $Ls$. The inductor $L$ starts to linearly discharge, and the clamped diode in Cell 6 is commutated. The resonant frequency $f_R$ in the step-down operation is the same as that in the step-up operation. Therefore, the current $iM$ flowing through the lower stack can be written as

$$i_M = i_L - i_N. \quad (11)$$

This analysis for step-down operation explains the current waveforms in Fig. 6. The inductor current has a sawtooth wave shape, and the lower stack current is zero during Mode 1. In Mode 1, the upper stack current is equal to the inductor current. In Mode 2, the upper stack current is discharging with a resonant wave shape, which, together with the inductor current, determines the lower stack current. To derive the step-down output voltage $vL$ as a function of charging ratio $d$ (defined in step-up operation) and high voltage $vH$, the inductor current $iL$ is assumed to be the same after one equivalent charging cycle. Similar to the step-up operation, it can be approximated that $NvCj = vH$. The conversion ratio can be derived as

$$\frac{v_H}{v_L} = \frac{N}{1 - d}. \quad (12)$$

The low voltage operation has the same step ratio function as that in the step-up operation. This means that the proposed modular multilevel dc–dc converter is similar to the conventional bidirectional dc–dc converter in terms of step ratio. By changing the current directions, the converter achieves bidirectional power conversion and the same step ratio without modifying the switching arrangement.

D. Capacitor Voltage Clamping Mechanism

This property can be explained by using the step-up operation for example. The converter has a cell capacitor voltage clamping mechanism. As is shown in Fig. 7(a), when the low-voltage-side inductor is charging (Mode 1), there are capacitors of Cell 1, Cell 2, Cell 3, and Cell 4 supporting the high-side dc voltage. Since the resonant tank formed by the cell capacitors and inductor $Ls$ has an impedance close to zero at the resonant frequency, the ac voltage drop across the resonant components is negligible.

Therefore, the output high voltage is almost equal to $vO = vC1 + vC2 + vC3 + vC4$. In the next operation mode [see Fig. 7(b)], the output voltage can be expressed as $vO = vC2 + vC3 + vC4 + vC5$. Hence, by comparing the two equations, it can be stated that $vC1 = vC5$. In the next operating cycle, using the same method, one can state that $vC2 = vC6$. The following operation mode sequence in the remaining switching cycle gives $vC1 = vC3 = vC5$ and $vC2 = vC4 = vC6$. The capacitor voltages of the upper cells are always clamped by the capacitor voltages of the lower cells.
Therefore, by balancing the two lower cell capacitors, the dc voltages of all the capacitors should be equal in steady state. For the converter with only one cell in the lower position, the circuit will have inherent balancing ability and does not even require additional balancing control. When needed, balancing control for lower cells can be used as shown in Fig. 9.

The reference cell voltage is calculated by averaging the capacitor voltages in half-bridge cells, i.e.,

$$v_{ref}^* = \frac{1}{N} \sum_{j=N+1}^{N+M} v_{cj}$$

with $v_{cj}$ as the sampled capacitor voltage. As capacitor voltages contain considerable ac components, first-order lowpass filters are used. By comparing the reference voltage with the dc voltage of each cell, a proportional feedback control is used for regulation. A dead zone is created to allow a small tolerance of voltage imbalance. A saturation function is used to limit the adjustable range. As the current at the switching instant, and in average is positive while the cell capacitor is connected in series to the others, this capacitor voltage can be charged by increasing the cell duty cycle.

The general output voltage feedback control for all submodules is shown in Fig. 10. The voltage regulator is represented by $H(v)$, usually an antiwindup proportional-integral controller or a phase lead controller. The gain in this controller for submodules in the lower position is doubled compared with that in the upper position because of the duty-cycle differences (see Fig. 5). The pulse generated by the lower submodules is almost complementary to that of upper submodules.

4. SIMULATION RESULTS

A downscaled simulated prototype with four upper cells and two lower cells was constructed based on the proposed circuit in Fig. 2(b) for verification. As a result, the resonant frequency was expected to be approximately 4.1 kHz. The submodules were implemented using capacitors with a nominal capacitance value of 50 μF. The switching frequencies for upper cells and lower cells were fixed as 1 and 2 kHz, respectively, giving an effective operational frequency of 4 kHz, which is slightly less than the resonant frequency. The complete circuit parameters are listed in Table I.

A. Open-Loop Tests

The open-loop tests used a fixed charging ratio of $d = 0.6$. For the step-up operation, the input voltage was 30 V, and the output voltage was expected to be 300 V. However, as the switches are not ideal, the high voltage will be lower than the expected value. For comparison purposes, the converter using the experimental parameters has been simulated. Fig. 12(a) and (b) shows the waveforms of simulated currents and voltages with voltage drop in each switch set to 1 V.

When the current $iN$ is negative in Mode 1, the voltage drop across the diodes is positive compared with $vN$. The experimental current and voltage waveforms are quite similar to the corresponding simulation results. However, when the current $iN$ in Mode 1 cross zero from negative, the current resonance is dramatically damped compared with the simulation result in Fig. 11 (the application example) where this current is freely resonating. This is caused by the voltage drop across the switches (which appears relatively large in this downscaled prototype).

When the current $iN$ changes to positive, the voltage drop across the IGBTs becomes negative compared with $vN$. Because in this mode the inductor L is charging and the capacitor CH is discharging, the rise of current $iN$ is suppressed until the end of this mode. When Mode 2 begins, the inductor current $iL$ is discharged to the high-voltage side, and the current $iN$ keeps resonating until it reaches zero or the end of the equivalent operating cycle.

The simulated stack voltage waveforms in Fig. 12(b) are close to the experimentally measured stack voltage waveforms. However, the upper-stack voltage $vN$ is lower than the expected amplitude. As a result, the conversion ratio is lower than 10:1. The output voltage
should be adjusted by closed-loop control to achieve the required level. The sum of the lower-stack voltage and upper-stack voltage is far below 300 V.

**TABLE I**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Quantity</th>
<th>Value</th>
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<tbody>
<tr>
<td>$V_{L}$</td>
<td>Nominal low dc voltage</td>
<td>30 V</td>
</tr>
<tr>
<td>$V_{H}$</td>
<td>Nominal high dc voltage</td>
<td>300 V</td>
</tr>
<tr>
<td>$I_{pk}$</td>
<td>Maximum switch current</td>
<td>30 A</td>
</tr>
<tr>
<td>$T_{s}$</td>
<td>Sampling period</td>
<td>100 μs</td>
</tr>
<tr>
<td>$T_{c}$</td>
<td>Equivalent operating cycle</td>
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</tr>
<tr>
<td>$I_{s}$</td>
<td>Low voltage side inductor</td>
<td>0.21 μH</td>
</tr>
<tr>
<td>$C_s$</td>
<td>Series capacitor</td>
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</tr>
<tr>
<td>$C_{Lo}$</td>
<td>Low voltage side capacitor</td>
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</tr>
<tr>
<td>$R_{hf}$</td>
<td>High voltage side load</td>
<td>1070 Ω</td>
</tr>
</tbody>
</table>

All the cell capacitors in the upper stack are in series with the inductor $L_s$, forming a resonant tank for $i_N$ to discharge. The stack voltage waveforms are in accordance with the waveforms in Fig. 6. This verifies the operation analysis of the proposed converter. The output high voltage is around 25 V with $v_H = 300$ V under open-loop control. The output voltage is lower than the expected value due to the voltage drop across the IGBTs.

**Fig. 12.** Simulation waveforms of the proposed converter for step-up conversion (X-axis: time, 50 μs/div). (a) Simulated currents (Y-axis: magnitude of current, 2 A/div). (b) Simulated voltages (Y-axis: magnitude of voltage, 100 V/div).

For low voltage operation, the input high voltage was set to 300 V. The output low voltage is expected to be 30 V. However, as there are voltage drops in the real switches, the output voltage may be lower than expected. Fig. 13(a) and (b) shows the simulated step-down current and voltage waveforms with 1-V voltage drop in each switch. In contrast, the experimental step-down current and voltage waveforms are quite similar to the relevant simulation results. The inductor $L$ is charging in Mode 1 and discharging in Mode 2. The currents $i_L$ and $i_N$ should linearly increase in Mode 1 and $i_L$ equals $i_N$. In Mode 2, the current $i_L$ starts to linearly decrease. The lower stack current is zero during this mode.

**Fig. 13.** Simulation and experimental waveforms of the proposed converter for step-down conversion (X-axis: time, 50 μs/div). (a) Simulated currents (Y-axis: magnitude of current, 2 A/div). (b) Simulated voltages (Y-axis: magnitude of voltage, 100 V/div). (c) Low voltage

**B. Linearity Tests**

Fig. 14 shows how the output (high-side) voltage varies as the input (low-side) voltage is changed for a fixed charging ratio of $d = 0.6$ (that is, open-loop operation) and also the characteristic of an ideal dc transformer. The linearity of the output voltage versus the input voltage of the step-up operation is tested. The circuit shows a linear relation between output and input voltages but with an offset compared with the ideal case. This offset is accounted for by the conduction voltage drops of the IGBTs and diodes of the submodules. The low submodule voltage in this downscaled prototype results in a noticeable relative error in Fig. 14 when the input voltage is particularly low.

**C. Closed-Loop Tests**

Closed-loop control was applied to test the regulation properties of the converter. The output voltages were fed back to change the charging ratio.
Fig 15. Simulation results of high voltage
Compared with the waveforms under open loop control with $d = 0.6$ (see Fig. 12), it can be seen that the charging ratio $d$ in the closed-loop curve has been raised by the controller. As a result, the step-up conversion ratio of 10:1 is achieved such that the high voltage $v_H$ is almost 300 V. Fig. 15 shows the measured step-up voltages under closed-loop control. It can be observed that the closed-loop controller is effective as the high voltage is always controlled around the rated value 300 V.

VI. CONCLUSION
The designed converter has the ability of bidirectional power flow control. A transformerless converter has been given and evaluated. The submodules are connected in series which supports the high voltage. The maximum output voltage operation and step-down operation are observed. This converter has the ability to operate under open loop control as a dc transformer with good linearity. Alternately, closed-loop control is also applied for trimming of the output voltage. The operating principle was verified by using bench scale experimental prototype. This converter may show relatively higher losses because of the high ac current that resonates in the submodules but considerably high efficiency was shown to be possible in high voltage applications. By increasing the level of submodules, further efficiency improvement can be achieved with lower switching frequency but cell capacitors with a higher volume will be required. The converter can attain a large step-up conversion ratio without the use of transformers. The proposed converter has the features of modularity, scalability, and simplicity and these may make it attractive in some special applications.

REFERENCES

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