Four-Level Dual Inverter Fed Induction Motor Drive
For Asymmetrical Efficient Control Strategy

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ABSTRACT - This paper presents modified control strategy for four-level Asymmetrical dual inverter fed induction motor drive. In this paper a modified control strategy for the dual inverter fed induction motor drive to improve performance in all the aspects at different modulation index when compared to the exiting control strategy. With the modulation index less than 0.3 the drive is operated such that minimum switching losses take place. With the modulation index in the range 0.3 to 0.6 common mode voltage is reduced. At modulation index greater than 0.6 both control strategies have same similarities. The total harmonic distortion is also reduced with modified control strategies at low modulation indices. The simulation based analysis is carried on scalar controlled dual inverter fed induction motor drive.

Index Terms—Dual Inverter; imaginary switching times; Space Vector Pulse width Modulation;

I INTRODUCTION

The output voltage of Voltage Source Inverter (VSI) contains harmonics. These Harmonics have adverse effect on the performance of the load (induction motor), as well as causes ripple in the phase currents. The harmonic current in the output voltage or current is determined by the Pulse Width Modulation (PWM) technique and switching frequency employed for inverter. Different PWM techniques were proposed in [1] to improve the quality of output voltage. Among various PWM techniques Space Vector Pulse Width Modulation (SVPWM) technique proposed in literature [2] has high DC utilization and low switching losses when compared with popular Sinusoidal PWM (SPWM). Implementation of SVPWM technique can be carried out in carrier based modulation approach and digital approach [3-4]. Conventional SVPWM proposed in paper [2-4] samples a given reference vector in a given sampling time Ts. The reference vector is sampled using active voltage vectors (V1 to V6) and zero voltage vectors (Vo & V7). The dwell time for which active voltage vectors and zero voltage vectors are applied for a time T1, T2 and Tz as given in (1).

\[
T_1 = \frac{V_{ref} \sin \left( \frac{\pi}{3} - \alpha \right)}{\sin \left( \frac{\pi}{3} \right)} \quad (1a)
\]

\[
T_2 = \frac{V_{ref} \sin(\alpha)}{\sin \left( \frac{\pi}{3} \right)} T_s \quad (1b)
\]

\[
T_z = T_s - T_1 - T_2 \quad (1c)
\]

The calculation of dwell times requires angle information and reference magnitude information. Therefore calculation of magnitude and angle in conventional SVPWM approach is complex and time consuming. Hence a simplified approach based on imaginary switching time is proposed in literature [5-7] to calculate dwell times. Using the concept of imaginary switching times the dwell times can be calculated and given by (2).

\[
T_1 = T_{an} - T_{bn}
\]

\[
T_2 = T_{bn} - T_{cn}
\]

\[
T_z = T_s - T_1 - T_2
\]

The imaginary switching times are calculated from the reference voltage vectors as in (3) [3]

\[
T_{an} = \frac{T_s}{V_{dc}} V_{an}
\]

\[
T_{bn} = \frac{T_s}{V_{dc}} V_{bn}
\]

\[
T_{cn} = \frac{T_s}{V_{dc}} V_{cn}
\]

Thus the complexity involved in calculation of dwell times is reduced. But the calculation of dwell times is also complex and time consuming. In this paper a simplified SVPWM algorithm is presented by simply
adding a zero sequence voltage to the commanded reference voltages.

With the proposed PWM algorithm to the three-phase two level VSI the output voltage and frequency can be controlled but harmonic content is still high in the output voltage or current. The harmonics can be reduced by increasing switching frequency. But with the increase in switching frequency, switching losses also increases. To achieve low harmonic in the output voltage at low switching frequency different multilevel inverter topologies like diode clamped, capacitor clamped and H-bridge topologies are presented in the literature [8-10]. As the number of levels increases the harmonic content in the output voltage gets reduced. But as number of levels increases complexity of circuit also increases. The diode clamped multilevel inverter can reduce the harmonic content in the output voltage but require clamping diodes which make the circuit complex and neutral point fluctuations are also present. Hence a new topology called H-bridge topology came into existence in which neutral point fluctuations are absent. But this circuit configuration requires separate voltage sources for each phase, which increases the number of sources.

A simple circuit configuration to generate three-level output voltage by using two two-level inverters is proposed in the literature [11] called as dual inverter. This dual inverter configuration is simple to implement. The dual inverter can overcome all the drawbacks of diode clamped and H-bridge multilevel inverter topologies. The dual inverter configuration can also be extended to higher levels [12-13] with the application of unbalanced input DC voltages to the dual inverter configuration as shown in Fig.I.

Fig. I Dual inverter circuit configuration with unbalanced voltage.

The authors in paper [13] proposed a control strategy for the dual inverter configuration. The conventional control strategy has high switching losses, high common mode voltages and high ripple in phase current at low modulation index. In this paper a modified control strategy is proposed which can reduce switching losses up to 50%. Along with reduction in switching losses, common mode voltage and current ripple is also reduced with the proposed control strategy.

II SIMPLIFIED SVPWM ALGORITHM

To generate the SVPWM modulating signals consider three reference signals as given in (4) and zero sequence voltage ($V_{zs}$) is added to the commanded reference signals as in (5)

$$V_a = V_m \cdot \cos(\omega t)$$
$$V_b = V_m \cdot \cos(\omega t - 120)$$
$$V_c = V_m \cdot \cos(\omega t - 240)$$

$$V_{ref} = V_{ref} + V_{zs}$$

Where

$$V_{zs} = \frac{V_{dc}}{2} (2a_0 - 1) = a_0 V_{max} + (a_0 - 1)$$

In conventional SVPWM algorithm zero state is divided into two equal halves between zero voltage vectors. So in simplified SVPWM algorithm $a_0$ is considered to be 0.5. By varying value of $a_0$ within the limit 0 and 1 various discontinuous PWM modulating signals can also be generated. But, this paper focuses on SVPWM algorithm only.

III. CONTROL STRATEGIES FOR DUAL INVERTER

Fig. I represents the dual inverter configuration with unbalanced input voltages ($2V_{dc3} \& V_{dc3}$). Where $V_{dc}$ represents the DC input voltage. $V_{ao}$, $V_{bo}$, $V_{co}$ are the corresponding pole voltages of inverter-I. $V_{a0}$, $V_{b0}$, $V_{c0}$ are the corresponding pole voltages of inverter-II. $V_{aa}$, $V_{bb}$, $V_{cc}$ are the effective pole voltages. $V_{ab}$, $V_{bc}$, $V_{ca}$ are the line voltages. With top switches are ON in inverter-I, it produces an output pole voltage of $2V_{dc3}$ and 0 when bottom switches are ON. Similarly inverter-II produces a voltage of $V_{dc3}$ and 0. With these inverter pole voltages, the possible effective pole voltages are given in Table: I. The effective pole voltages are given by (6). The configuration is capable of generating 4-level output pole voltage

$$V_{aa} = V_{a0} - V_{a0'}$$
$$V_{bb} = V_{b0} - V_{b0'}$$
$$V_{cc} = V_{c0} - V_{c0'}$$

(6)
Carrier based modulating approach is adapted for the proposed dual inverter configuration. Multi level carrier based modulating approach requires \( N-1 \) triangles to generate \( N \) level output voltages. The proposed inverter configuration is capable of generating four-level output voltage. So carrier based modulation approach requires three triangles. The modulating wave is having peak amplitude of \( V_{m^*} \) and frequency (1) The peak amplitude of modulating wave lies between 0 and 1. The carrier wave is having amplitude of \( V_c \) and frequency of \( f_{sf} \) (switching frequency). The amplitude of carrier wave and modulation index (\( M \)) of modulating wave is given by (7)

\[
V_c = \frac{1}{N-1} \quad (7a)
\]

\[
M = \frac{\pi V_{ref}}{2V_{dc}} \quad (7b)
\]

modulating signal present in region RI as shown in Fig. 3 only one inverter (Inverter-II) is in operation and produces an output voltage of \( (0, V_{dc}/3, 2V_{dc}/3) \) which is considered as two-level output voltage.

If modulating signal is present in all the three regions as shown in Fig. 4 both inverters are in operation but the inverters are operated such that it generates four level output voltage of \( (0, V_{dc}/3, 2V_{dc}/3, V_{dc}) \).

IV. SIMULATION RESULTS AND DISCUSSION

To validate the proposed control strategy MATLAB based simulation analysis are carried out. The Simulation parameters used in the induction motor drive are given in table-II. The simulation results at different modulation indices are shown in Fig.

<table>
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<td>Table 3: Comparison of THD's</td>
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With modulation index less than 0.3, in convention SVPWM based control strategy both inverters are in operation. Along with the reduction of switching losses and common mode voltage at different modulation index with proposed control strategy the current ripple is also affected with different control strategy.

<table>
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The total harmonic distortion of line current at different modulation indices with two control strategies are tabulated in Table-III and it is observed that current THD at low modulation is low with the proposed control strategy. As modulation index increases the amount of harmonics present in the phase currents is also reduced because of increase in levels of voltage. At high modulation index both control strategies have same current ripple.

V. CONCLUSION

The dual inverter configuration with unbalanced input voltage is having less complexity when compared to other multilevel inverter topologies. With the convention control strategies at low modulation indices (less than 0.3) the dual inverter configuration is having high switching losses because of operation of both inverters. But with the proposed control strategy nearly 50% of switching losses are reduced as only one inverter in operation. In the modulation index range 0.3 to 0.6 common mode voltages are reduced because of low effective pole voltage. At high modulation index (greater than 0.6) both control strategies have same effects. Along with the reduction in switching losses and common mode at low modulation index, current ripple is also reduced with the proposed control strategy.

REFERENCES