IMPLEMENTATION OF AREA EFFICIENT FFT/IFFT PROCESSOR FOR MIMO OFDM SYSTEMS

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ABSTRACT:

The FFT/IFFT processor is widely used in various areas such as 4G telecommunications, speech and image processing, medical electronics and seismic processing, etc. In this paper an efficient implementation of FFT/IFFT processor for multiple input multiple output-orthogonal frequency division multiplexing (MIMO-OFDM) systems with variable length is presented. This paper opts memory scheduling and Multipath Delay Commutator (MDC) as the hardware architecture. Radix-Ns butterflies are used at each stage, where Ns denote the number of data streams, so that there is only one butterfly is used in each stage. For area and time optimization and to reduce power consumption, the Read Only Memories (ROM‟S) which is used to store twiddle factor is replaced by complex multiplier. The design reduces the use of logic elements to 2.21% from 10.46% and achieves a maximum clock set up time of 3.981ns (251.19MHz) and worst case Tco of 49.314ns. The result shows the advantages of the proposed scheme in terms of area and power consumption

Keywords: Fast Fourier transform (FFT), Memory scheduling, Complex multiplier, MIMO, OFDM.

I. INTRODUCTION

FFT is an important element in Orthogonal Frequency Division Multiplexing (OFDM) system. It is a method of encoding digital data on multiple carrier frequencies. Multi Carrier Modulation is the base of OFDM, where high-rate data stream is splitted into number of lower rate data streams and they are transmitted simultaneously over a number of subcarriers. OFDM has been used in wide range of applications from wired communication modems, such as
Digital subscriber line (xDSL) to wireless communication modems such as WiMAX, 3GPP, Long term evolution (LTE) to process baseband data. The reliability of Orthogonal Frequency Division Multiplexing (OFDM) makes it favorable to adopt in broadcasting applications such as Digital Audio Broadcasting (DAB).

Multiple Input Multiple Output (MIMO) systems are devices that are used in wireless communication. These are devices consisting of array of transmitters and receivers. With MIMO device it is possible to obtain high data. Hence combination of MIMO and OFDM system provides promising data rate and reliability in wireless communications.

Fast Fourier Transform (FFT) is an efficient algorithm proposed by Cooley and Tukey to compute Discrete Fourier transform (DFT) which converts time to frequency and reduces the time complexity to O(N log 2N), where N denotes the size of FFT[2]. For the purpose of hardware implementation, various FFT processors have been used mainly memory based and pipeline architecture. Memory based architecture cannot be parallelized where as the pipeline architecture can overcome the disadvantages of the former architecture. Generally, the pipeline FFT processors is classified in two design-Single-path delay feedback (SDF) pipeline architecture, and Multiple-path delay Commutator (MDC) pipeline architecture[5].Single path delay feedback (SDF) reduces amount of multipliers but it complicates the control mechanism and uses more memory resources whereas Multipath Delay Commutator saves more area,[5] and thus MDC is adopted as the hardware architecture. Multipath Delay Commutator (MDC) makes the feedback paths in to feed forward streams using switch boxes along with memory. In this paper Multipath Delay Commutator and memory scheduling is used to implement fast Fourier transform for multiple input multiple output orthogonal frequency division with variable length. But for computation of FFT we need to use twiddle factor to multiply with input signals to obtain output, and for this a large size of ROM is needed to store twiddle factors which in turn increases the cost. Thus for further improvement, ROM-less FFT/IFFT processor which eliminates ROM‟s that store twiddle factor is presented. The complex

multipliers are used for this purpose and they perform shift-and-add operations, thus the processor uses a two-input digital multiplier and does not need any ROM to store twiddle factor [2]. Thus the proposed architecture also includes a reconfigurable complex constant multiplier to store twiddle factor instead of using ROM‟s.

II.LITERATURE SURVEY

FAST Fourier transform (FFT) is the major block in orthogonal frequency division multiplexing systems. Ofdm has allocated in a large range of applications from wired-communication modems, such as digital subscriber lines (xDSL) [1], [2], to wireless-communication modems, like IEEE802.11 [3] WiFi, IEEE802.16 [4], [5] Wi MAX or 3GPP long term evolution (LTE), to process baseband data. Inverse fast Fourier transform (IFFT) converts the modulated information from frequency domain to time domain for transmission of radio signals, while FFT gathers samples from the time domain, again converting them to the frequency domain.

Y.G.Li, J.H. Winters and N.R.Sollenberger[6] proposed multiple input multiple output (MIMO) devices, data throughput can be increased drastically. Hence MIMO-OFDM systems provide data rate and reliability in wireless communications. To handle “multiple” data streams, firstly the functional are to be duplicated for processing the giveninputs. Without a proper design, the complexity of FFT/IFFT processors in MIMO systems increases linearly with the number of data streams.

B. G. Jo and M. H. Sunwoo [8] proposed pipelines schemes, are the architectures most widely adopted for the
implementation of FFT/IFFT. From the memory access perspective, in-place memory updating schemes performs the computation in three phases: writing in the inputs, updating intermediate values, and reading out the results. In updating phase, the processor reuses the radix-r processor, such that a single radix-r butterfly is sufficient to complete N-point FFT/IFFT computation. Since each phase is non-overlapped, the outputs can be sequential or as requested. However, it is the non-overlapping characteristic that makes the butterfly idle in memory write and read phases, and the overall process is lengthy. Continuous-flow mixed radix (CFMR) FFT.

P. Y. Tsai and C. Y. Lin [9] utilizes two N-sample memories to generate a continuous output stream. One of the memories is used to calculate current FFT/IFFT symbols, while the other stores the previously computed results and controls the output sequence. Thus, when CFMR is used in MIMO systems, the required memory is increased in a trend proportional to 2×Ns, where Ns is the number of data streams. Such memory requirement may be forbidden if Ns is large, because the area of memory does not shrink as much as that of logic gates when fabrication technology advances, due to the use of sense amplify circuitry.

III.FFT/IFFT PROCESSORS

Fast Fourier Transform and Inverse Fast Fourier Transform are the most efficient and fast algorithms to calculate the Discrete Fourier Transform and Inverse Discrete Fourier Transform respectively. Fast Fourier Transform/Inverse Fast Fourier Transform is mostly used in many communication applications like Digital Signal Processing and the implementation of this is a growing research. From the last years, OFDM became an important one in FFT/IFFT algorithms and is going to be implemented.

The efficient multiple access method for Bandwidth in digital communications is OFDM (Engels, 2002; Nee & Prasad, 2000). Many of nowadays OFDM technique can be used in most important wireless communication systems: Digital Audio Broadcasting (DAB) (World DAB Forum, n.d.), Digital Video Broadcasting (DVB) , Wireless Local Area Network (WLAN) , Wireless Metropolitan Area Network (WMAN) and Multi Band –OFDM Ultra Wide Band (MB–OFDM UWB). Moreover, this method is also utilised in important wired applications like Asymmetric Digital Subscriber Line (adsl) or Power Line Communication.

Every communication system must have both Transmitter and Receiver. At the Transmitter side, IFFT is used for modulating signal, which depends on the OFDM system and at the Receiver side, FFT is used for demodulating signal.The FFT/IFFT are the important modules in OFDM transceivers. From this we can say that, the most parts of OFDM systems are, IFFT can be used at the transmitter side where as viterbi decoder can be used at the receiver side (Maharatna et al., 2004). The FFT is the second calculative huge block at the receiver section.

The fft and ifft must be implemented such that to achieve the required throughput with the reduced area and delay.

The modern ofdm transceivers requirements may lead to the implementation of special hardware, which is the critical block in the transceiver. Hence the fft/ifft can be implemented as a Very Large Scale Integrated circuit.

The methods that we applied to the FFT can also be applied to the IFFT. From the output of a FFT processor, we can easily get the ifft. Therefore, the discussion in this chapter concentrates on the FFT without loss of generality.

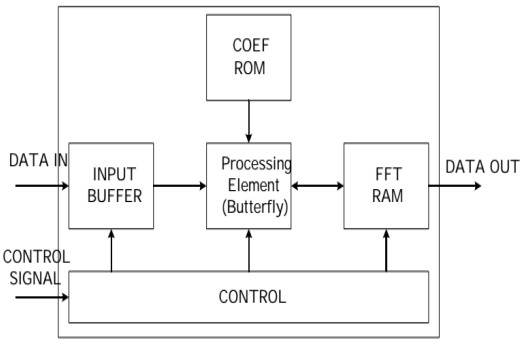

Fig1. Internal architecture of FFT/IFFT processors

IV. MDC ARCHITECTURE FOR MIMO FFT/IFFT

Storage elements dominate most of the area in conventional MDC architecture. That is, the input buffering stage for radix-4
based FFT/IFFT needsN/4+N/2+3N/4 words of memory, and each computing stage needs 3N/4 s words of memory, wheres is the stage index. For a 2048-point MDC FFT/IFFT processor, 5112 words of memory are required. If MDC is applied in MIMO-OFDM systems, the memory size grows linearly with the number of data streams. As for the utilization rate of butterflies and multipliers, since 3/4 of the computing time is used to gather the input data, the utilization rate is only 25% in single stream radix-4 MDC FFT/IFFT. Although MDC architecture offers an intuitive and simpler data flow control, most of the previous works use SDF instead of MDC for complexity concern. However, for MIMO FFT/IFFT, we found that if the data streams are properly scheduled, the utilization rate can increase from 25% to 100%. This makes MDC very suitable for MIMO-OFDM systems.

Therefore we propose an efficient mechanism of memory scheduling to reduce the required memory. Together with the proposed memory scheduling, the proposed MIMO MDC FFT/IFFT has the following advantages. First, the proposed memory scheduling mechanism reduces the size of storage elements. Moreover, the mechanism properly shuffles the four input streams such that stage one to stage five are all with the same feed-forward switch-box data flow. Therefore, the control simplicity of MDC schemes can be preserved whilethe memory size is greatly reduced. As for the utilization
rate of butterflies and multipliers, each one of the four input symbols after memory scheduling takes 25% of one symboltime for radix-4 butterfly computation. Consequently one radix-4 butterfly and three twiddle-factor multipliers in each pipeline stage can process four data streams without any idle period, that is, the utilization rate of butterflies and multipliers is 100%. Furthermore, the radix-8 butterfly at the last stage can be configured as a radix-4 butterfly. With such flexibility, radix-2 computation can be incorporated at the last radix-8 stage, and thus for any N in power-of-2 fashion can be computed with this proposed method. Finally, the serial blocks of output symbol format helps to reduce the memory usage for output sorting and the complexity of the modules followed by the FFT/IFFT processor.

V ALGORITHM FOR PROPOSED ARCHITECTURE

For description convenience, the following notations are applied:i stands for spatial stream index, j stands for OFDM symbol index,nstands for input sample index, andkstands for output sample index. Thus each input sample can be represented as xij[n]. Moreover, s denotes the pipeline stage, ranging from one to five in the proposed design. Fig. 2 shows the block diagram of the proposed MIMO FFT/IFFT computing core with N =2048. The input order and the indices in between are also annotated.

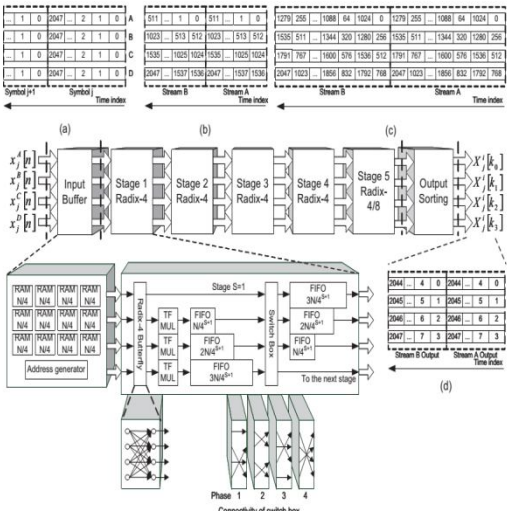

Fig. 2. Block diagram of the proposed MIMO MDC FFT/IFFT processor. The routing rule updates every N/4s+1clock cycles. (a) Initial input order.(b) Sorted input order at the output of input buffer. (c) Computed output order without sorting. (d) Output order after output sorting

The Fast Fourier transforms (FFT) and its inverse (1FFT) is one of the fundamental operations in digital signal processing (DSP). The FFT/IFFT is widely used in various areas such as telecommunications, speech and image processing, medical electronics and seismic processing, etc. Recently, the FFT/IFFT is used as one of the key component in MIMO -based wideband communication systems, like xDSL modems. An FFT processor can be implemented as memory based single butterfly architecture or pipeline architecture. The single butterfly architecture requires less hardware resources, but

its power consumption is higher as it operates at higher clock frequency to perform all the necessary butterfly operations. Therefore, pipeline architecture is generally preferred as they possess low power consumption.

The N-point FFT and IFFT are calculated as

$$X[k] = FFT\{x[n]\} = \sum_{n=0}^{N-1} x[n] W_N^{nk} \quad (1)$$

$$x[n] = IFFT\{X[k]\} = \frac{1}{N}\sum_{k=0}^{N-1} W_N^{-nk} \quad (2)$$

Where,

$$W_N^{nk} = cos(\frac{2\pi nk}{N}) - j\, sin(\frac{2\pi nk}{N}) \quad (3)$$

The IFFT can be realized by modifying the FFT which is given by equation (4)

$$x[n] = \frac{1}{N}(FFT\{X^*[k]\})^* \quad (4)$$

Usually N is a power of 2 and implementation of 1/N only involves right shift operation. Therefore, the IFFT share the same hardware with FFT .For these two systems, there are four FFT/IFFT lengths, that is, N = 2048,1024, 512, and 128 .Here let us take N=2048.In MDC , most of the area is
obtained by storage elements , that is, the input buffering stage for radix-4 based FFT needs N/4+ N/2+3N/4 words of memory, and each computing stage needs 3N/4s words of memory, where s represents the stage index. According to
this, 2048-pointMDC FFT/IFFT processor, 5112 words of memory are needed. If MDC is used in MIMO-OFDM systems, memory size grows linearly as the number of data stream increases. Even though MDC architecture provides simple control for data flow, most of the previous works use SDF instead of MDC for complexity concern. But if the data streams are properly scheduled, the utilization rate can be made full. This makes MDC suitable for MIMO-OFDM systems.

VI. RESULTS AND COMPARISON

Code development, synthesis, analysis related to timing and power for the proposed MDC FFT PROCESSOR with variable length for OFDM are carried out in Altera and simulation is done in ModelSim.

Synthesis output:

RTL Output and Compilation Report:

The RTL output for stage 1 of the processor and the overall RTL out for the MDC FFT Processor is shown in Fig.4 and
Fig.5 respectively. The synthesis output shows that the proposed ROM Less MDC FFT processor achieves 2.2% of total logical elements and 2.2% of total combinational fuctions, which was 10.46% for MDC FFT processor with ROM[3].The compilation report for the proposed processor is shown in Fig.3.

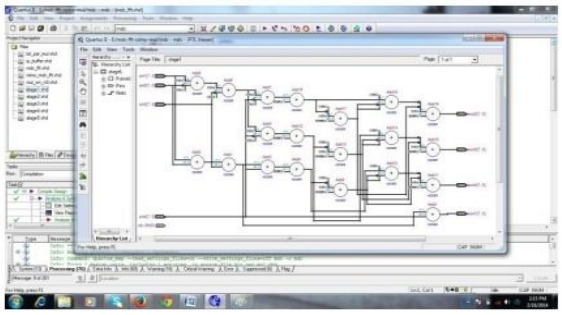

Fig 3: RTL Output of Stage 1

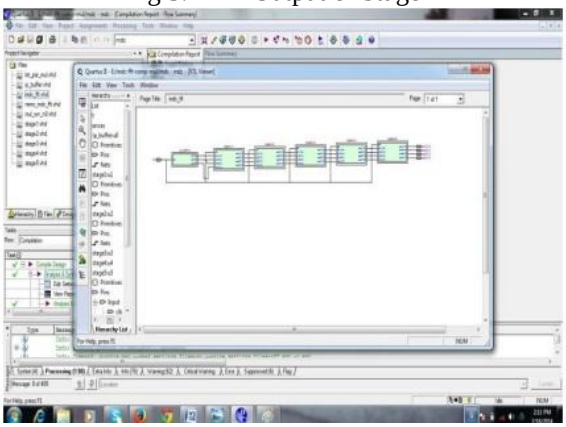

Fig 4: Overall RTL Output for Proposed Processor

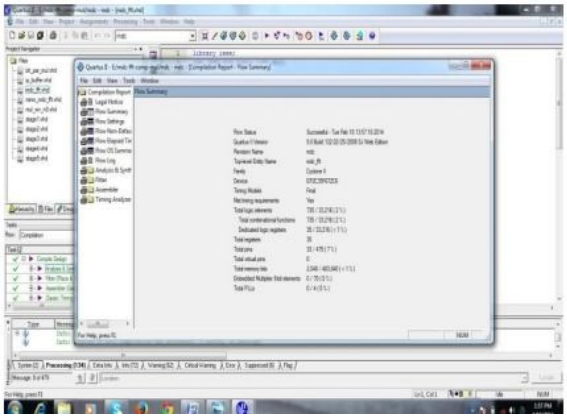

Fig 5: Compilation Report of MDC FFT Processor.

Timing analysis

The proposed system with complex multiplier achieves a maximum clock set up time of 3.981 ns(251.19MHz) and worst case Tcoof 49.314 ns which was 3.986ns (250.82MHz) and 64.228ns respectively for

the processor with ROM. The timing analysis report for proposed MDC FFT processor is shown in Fig.6.

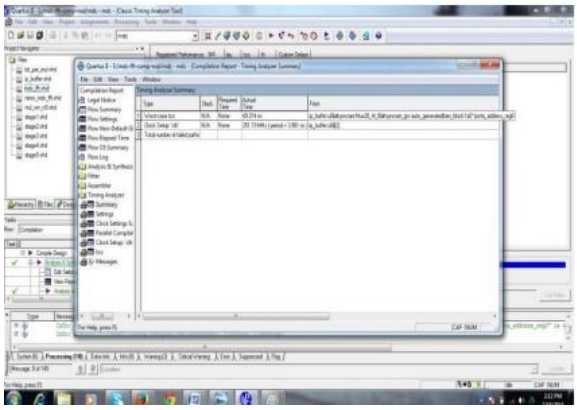

Fig 6: Timing Analysis Report

Power analysis

The power analysis report for proposed system is shown in Fig.7.The processor consumes a total thermal power of 113.89mW which includes core static thermal power dissipation of 79.94mW, core dynamic static thermal power dissipation and I/O thermal power static dissipation of 33.95mW

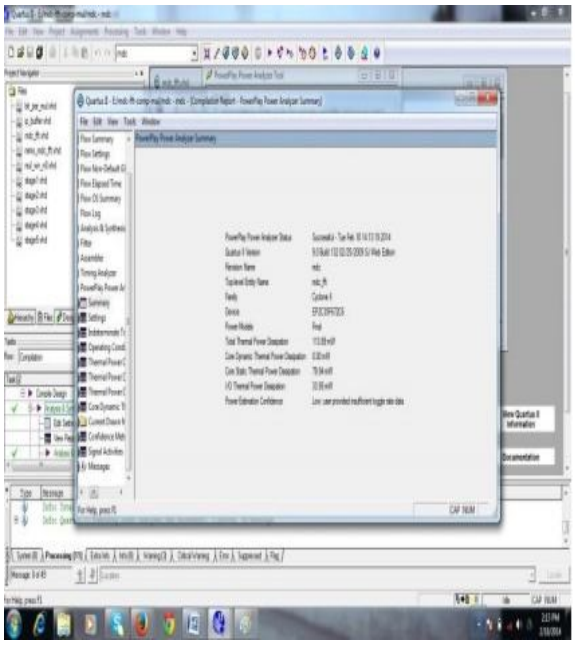

Fig 7: Power Analysis Report.

Simulation output:

The proposed MDC FFT Processor simulation was carried out in Altera ModelSim and the waveforms are shown in the Fig 8. The inputs are given to the processor through the input pins sin1, sin2, sin3, sin4. Similarly, clock pulse is given through „clk" pin. The Outputs for the processor are taken from sout1, sout2, sout3, sout4.

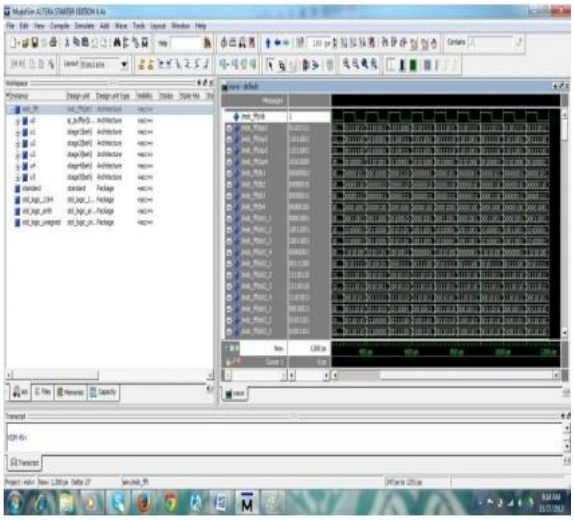

Fig 8: Simulation Output

CONCLUSION

In this paper, a ROM less radix-r based MDC MIMOFFT/IFFT processor for processing Ns streams of parallel inputs is proposed. The proposed technique is preferable for MIMO-OFDM baseband processor such as WiMAX [8] or LTE applications. The efficient memory scheduling and constant complex multiplier considerably decreases the chip area because the memory requirement usually dominates the chip area in an FFT/IFFT processor. Therefore, we conclude that the proposed design optimizes area and energy efficient.

6. REFERENCES

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